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Restricted-Access Al-Mediated Material Transport in Al Contacting of PureGaB Ge-on-Si p^+n Diodes

AMIR SAMMAK,[1] LIN QI,[1] and LIS K. NANVER [2,3,4]

1.—Department of Microelectronics, Delft University of Technology, Delft, The Netherlands. 2.—Department of Physics and Nanotechnology, Aalborg University, Ålborg, Denmark. 3.—Semiconductor Components, MESA+ Institute for Nanotechnology, University of Twente, Enschede, The Netherlands. 4.—e-mail: ln@nano.aau.dk

The effectiveness of using nanometer-thin boron (PureB) layers as interdiffusion barrier to aluminum (Al) is studied for a contacting scheme specifically developed for fabricating germanium-on-silicon (Ge-on-Si) p^+n photodiodes with an oxide-covered light entrance window. Contacting is achieved at the perimeter of the Ge-island anode directly to an Al interconnect metallization. The Ge is grown in oxide windows to the Si wafer and covered by a B and gallium (Ga) layer stack (PureGaB) composed of about a nanometer of Ga for forming the p^+ Ge region and 10 nm of B as an interdiffusion barrier to the Al. To form contact windows, the side-wall oxide is etched away, exposing a small tip of the Ge perimeter to Al that from this point travels about 5 μm into the bulk Ge crystal. In this process, Ge and Si materials are displaced, forming Ge-filled V-grooves at the Si surface. The Al coalesces in grains. This process is studied here by high-resolution cross-sectional transmission electron microscopy and energy dispersive x-ray spectroscopy that confirm the purities of the Ge and Al grains. Diodes are fabricated with different geometries and statistical current–voltage characterization reveals a spread that can be related to across-the-wafer variations in the contact processing. The I–V behavior is characterized by low dark current, low contact resistance, and breakdown voltages that are suitable for operation in avalanching modes. The restricted access to the Ge of the Al inducing the Ge and Si material transport does not destroy the very good electrical characteristics typical of PureGaB Ge-on-Si diodes.

Key words: Pure B, pure Ga, Ge-on-Si, Ge diodes, photodiodes, Al-induced material mediation

INTRODUCTION

Germanium (Ge) has unique properties which make it a promising material in many different applications in the semiconductor industry including infrared sensors/imagers and high carrier mobility complementary metal–oxide–semiconductor (CMOS) electronics. In Ge, like in other semiconductor systems, a robust and low-ohmic metal contacting[1] is needed for the successful fabrication of (opto-)electronic devices. However, critical technological hazards posed by the diffusion of the contacting metal into the Ge to form large aluminide or germanide clusters[2] and also the high Schottky barrier height of n-type Ge to metals[3] continue to present problems in need of solutions. In Ge photodiode fabrication, nickel (Ni) can, for example, be used as a barrier/contacting metal together with gold (Au) to achieve low contact resistance.[4]

In this paper, the use of nanometer-thin pure boron (PureB) layers as interdiffusion barrier to aluminum (Al) metallization is investigated for the fabrication of p^+n infrared Ge photodiodes with a layer stack of silicon oxide (SiO_2), PureB and pure gallium (PureGa) as light-entrance windows. As an

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interconnect material in integrated silicon (Si) circuits, aluminum (Al) is the most commonly used material due to the processing versatility particularly with respect to patterning. However, Al readily reacts with Ge even at temperatures well below the eutectic temperature of about 420°C[5], and hence, a barrier layer is necessary. When working with Al as interconnect layer, a titanium/titanium nitride (Ti/TiN) layer stack has been demonstrated as contacting/barrier layer before depositing Al.[6] The use of the layer stack of PureB on PureGa, a combination known as PureGaB, as a contacting and barrier layer to Al is particularly attractive because it simultaneously creates an ultrashallow p^+n junction the low dark current of which was already demonstrated in our previous papers.[7–9] The photodiode anode region was realized by depositing the PureGaB directly on Ge islands grown on silicon wafers with all depositions performed in one and the same chemical-vapor deposition (CVD) reactor system. Both Ga and B are categorized as p-type dopants for group IV semiconductors. On Si, both PureB and PureGa depositions have been shown to provide a p^+-region for ultrashallow p^+n diodes with saturation currents as low as those of conventional diffused junctions.[10,11] Surprisingly, this is even the case for deposition temperatures down to 400°C where no p-doping of the bulk Si is expected. This has been accorded to the interface properties created by B-Si and Ga-Si bonds.[12] On Ge, the combination of first PureGa deposited at 400°C to create a p^+ region and then PureB at 700°C to enable reliable contacting with Al proved to be a practical way of achieving reliable low-saturation-current, I–V characteristics.[8]

For application as infrared photodiodes, avoiding Al directly above the photosensitive region is beneficial for the optical sensitivity. A process flow that allows this is examined here where a direct but small contact point between the Al and Ge is created at the Ge island perimeter. This leads to a significant but electrically nondestructive migration of Al through the Ge. This Al migration also results in pitting of the Si substrate. Although a number of prior studies in the literature have been devoted to Al-mediated recrystallization of Ge and SiGe alloys on foreign substrates including Si,[13–16] we found only one previous report of similar pitting behavior by Dale et al,[17] who concluded that the presence of a small percentage of Ge in an Al metallization on Si causes pitting by lowering the solubility of Si in the Al. In the process described here, Al/Si (1%) is employed, and normally this is enough Si-content to saturate the Al and prevent spiking of the Si substrate. However, even with the very restricted access of the Al to the Ge in our structures, there is a surprisingly large amount of material displacement of all three elements, the Ge, Al, and the Si. In addition to statistical electrical evaluations, this process is studied by high-resolution cross-sectional transmission electron microscopy (TEM) and energy dispersive x-ray spectroscopy (EDS). While the present paper focuses on the material-related behavior of the contacting scheme, the optical performance of these devices, also in avalanche operation mode, is presented in the paper[18] and shows enhanced near-infrared (NIR) responsivity as expected for Ge photodiodes.

EXPERIMENTAL PROCEDURES

A schematic of the fabrication process of the Ge-on-Si p^+n diodes is shown in Fig. 1 for (a) a diode covered with Al deposited directly on the PureGaB[7,8] and (b) a diode where the PureGaB is covered with an infrared-transparent silicon oxide and then contacted through windows etched at the diode perimeter.[9] The starting material is n-type Si (100) wafers. First, a 30-nm thermal SiO_2 followed by a 1-μm low-pressure CVD (LPCVD) SiO_2 is grown on the surface of the Si substrate. The SiO_2 layer is then patterned to open square windows with sizes 5 $\mu m^2 \times 5$ μm^2, 12 $\mu m^2 \times 12$ μm^2, and 26 $\mu m^2 \times 26$ μm^2. Three different types of devices are studied here with the same total area of 26 $\mu m^2 \times 26$ μm^2 but composed of different numbers of diodes as specified in Table I. The samples are then transferred to the CVD reactor, which is a commercial ASM Epsilon 2000 for Si/SiGe epitaxy that is especially equipped with a trimethylgallium (TMGa) bubbler system for deposition of Ga.[19] To grow the PureGaB Ge structure, the deposition cycle consists of a series of steps performed at different temperatures. First a less than 50-nm-thick selective Ge is deposited at 400°C to form a smooth, flat seed layer on the interface; then Ge deposition continues at 700°C with *in situ* arsenic n-doping and a higher deposition rate to achieve a thickness of between 0.6 μm to 1.6 μm with a doping level of $\sim 10^{16}$ cm^{-3}. The depo-

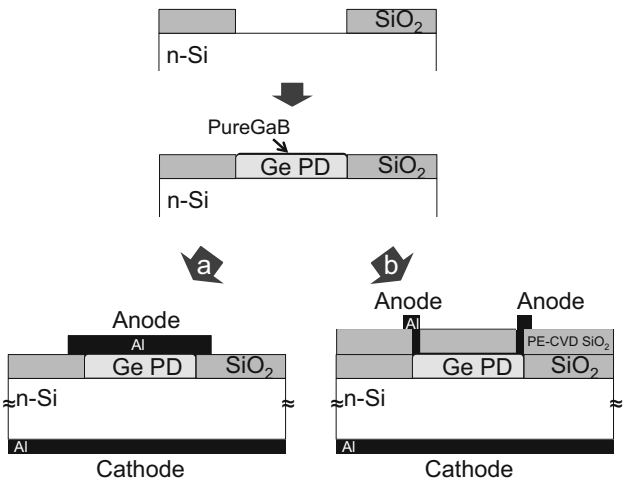

Fig. 1. Schematic process flow for the fabrication of PureGaB Ge-on-Si diodes with two different metallization methods: (a) contacting of the whole Ge diode surface by depositing Al directly on the PureGaB, and (b) fabrication of a central oxide light-entrance window by Al-contacting the Ge diode through a ring-shaped window to the PureGaB at the perimeter of the diode.

sition rate is highly dependent on the size and surrounding oxide area of each opening as well as the global percentage of open area across the wafer. The rate can vary between 50 nm/min and 100 nm/min at 700°C. Keeping the wafers in the reactor, they are given a 1-h anneal at 750°C which reduces the dislocation density in the Ge down to $\sim 10^7$ cm^{-2}.[20] After this step, without breaking the vacuum, a nm-thin layer stack of first Ga, and then B is deposited to form the p^+n junction on the Ge as described in Ref. 7 and 8. The solid solubility of B in Ge is considerably lower than that of Ga,[21,22] and in our experiments, PureB alone did not give a satisfactory result, whereas adding PureGa did. On its own, the PureGa is very unstable. It can react with the Ge and Al but will also oxidize as soon as the wafers are exposed to air. A much more reliable situation is created by covering it with PureB. As with the Ge deposition, the PureB thickness is susceptible to local and global loading effects. However, due to a high mobility of the boron across the wafer surface before it is adsorbed, the thicknesses across small windows close to each other on the wafer will be the same.[23]

Two approaches were taken for metallization of Ge-on-Si diodes. In the first approach, shown in Fig. 1a, 675-nm Al/Si(1%) is sputtered directly onto the diodes and then patterned as interconnect to give separate access to the anode of each of the diodes.[7] In the second approach as illustrated in Fig. 1b, first, a 1-μm-thick layer of plasma-enhanced CVD (PECVD) SiO_2 is deposited on top of the devices and then patterned with a ring-shaped opening around each diode. Next, 900-nm Al/Si(1%) is sputtered and patterned so that the central region of the diodes is only covered with oxide. The process is finished in both approaches by 30 min alloying at 400°C. In Fig. 2, three top-view SEM images are shown of the three different designs (listed in Table I) made with the metallization as shown in Fig. 1b.

RESULTS

A cross-sectional TEM image of a PureGaB Ge-on-Si diode fabricated with full metal coverage as depicted in Fig. 1a is shown in Fig. 3. The mushroom shape of the Ge with a thickness of 1.6 μm is due to overgrowth of the oxide. The PureGaB layer is seen to be conformal over the whole Ge surface independent of crystal orientation. The thickness is approximately 25 nm. Some parts appear to be much thicker, but this is believed to be an artifact of the sample thinning process because other experi-

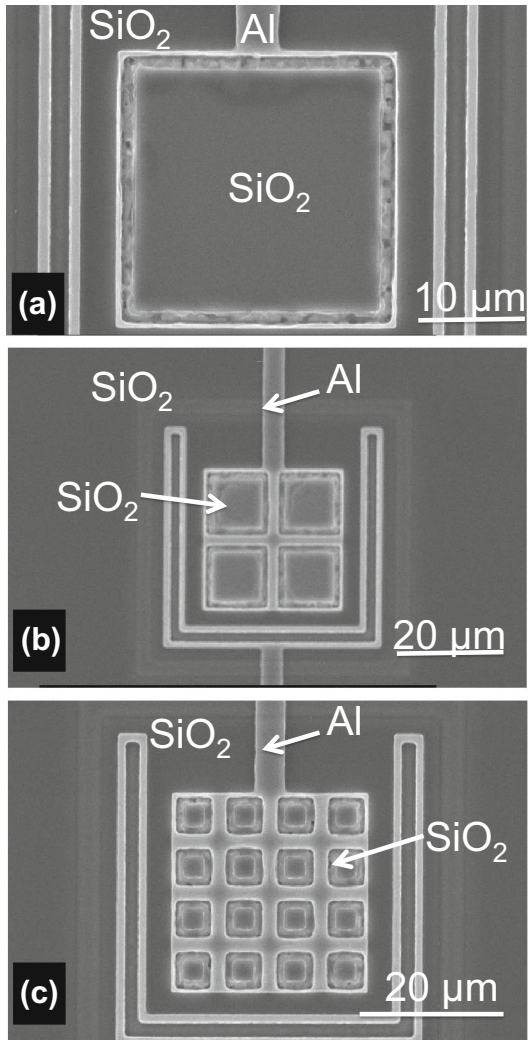

Fig. 2. Top-view SEM images of PureGaB Ge-on-Si devices fabricated with the metallization approach as shown in Fig. 1b for (a) a single-diode device of size 26 μm^2 × 26 μm^2, (b) a 4-diode device composed of 12 μm^2 × 12 μm^2 diodes, and (c) 16-diode device composed of 5 μm^2 × 5 μm^2 diodes.

Table I. Geometrical parameters of the 3 devices composed of different numbers of Ge diodes with the metallization made as shown in Fig. 1b, along with the lowest measured current values out of at least 100 measured devices of each type

	No. of diodes	Diode size (μm)	Total device area (μm^2)	Total Ge diode area (μm^2)	Total Ge diode perimeter (μm)	Current at 0.2 V forward bias (A)	Current at −2 V reverse bias (A)
Single-diode device	1	26 × 26	26 × 26	676	104	6.8×10^{-8}	7×10^{-11}
4-diode device	4	12 × 12	26 × 26	576	192	4.4×10^{-8}	5×10^{-11}
16-diode device	16	5 × 5	26 × 26	400	320	2.1×10^{-8}	2×10^{-11}

ments with PureB deposition reveal a very constant deposition rate. It is clear the PureB prevents interdiffusion between the Al metal and Ge. Photodiodes fabricated in this way, but with a thinner Ge-island to give a flat surface, have been presented in Ref. 7 that includes optical characterization showing high infrared sensitivity. They have low dark current and when operated as single photon avalanche diodes (SPADs) in Geiger mode, they display low dark-count-rate. This evidences that the Ge has a low defect density.

TEM images of devices made with the approach of Fig. 1b are shown in Fig. 4a and b for a 26 μm$\times$ 26 μm^2 and a 5 μm^2 $\times$ 5 μm^2 diode, respectively. A close-up is shown in Fig. 4c of the region around the 1-μm-wide contact window. From these TEMs, the PureB layer is estimated to be about 10 nm thick. From the extensive research on PureB Si diodes, it is known that a 2–3-nm-thick layer of PureB is thick enough to form a good interdiffusion barrier between Al and Si.[24] Such thin layers that allow tunneling are necessary for achieving low series resistance in micrometer-sized windows because the PureB layers have very high resistivity of more than 500 Ω cm.[25]

For the devices in Fig. 4a and b, the critical step was the etching of windows in the PECVD oxide. To maximize the purely oxide-covered Ge area for infrared sensing, the contact window is designed just inside the perimeter of the Ge island. A similar strategy was used for contacting of the PureB Si SPADs presented in Ref. 26. In that case, a plasma-etching step ending with wet HF dipping was used to selectively remove the oxide on the PureB. In the present process, only plasma etching with soft landing gave good results. However, the devices in Fig. 4a and b are seen to suffer from Al migration into the Ge, which also resulted in the displacement of Ge to form Ge-filled V-groove pits in the Si. The Al is seen to coalesce into grains within the Ge region. Both these grains and the V-grooves are visible at distances up to 5 μm from the diode perimeter. As is, for example, clear from Fig. 4c, close inspection of the Ge and oxide topography at the diode perimeter

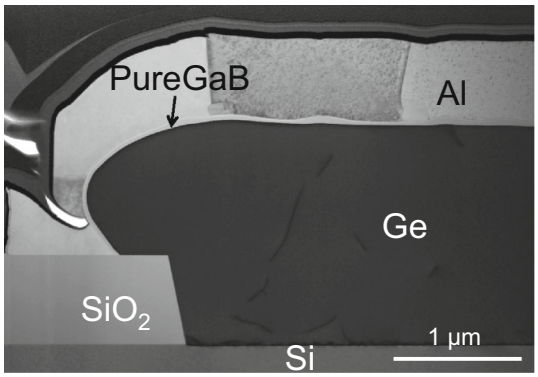

Fig. 3. TEM image of a Ge-on-Si diode fabricated as in Fig. 1a with Al-metallization directly on the PureGaB.

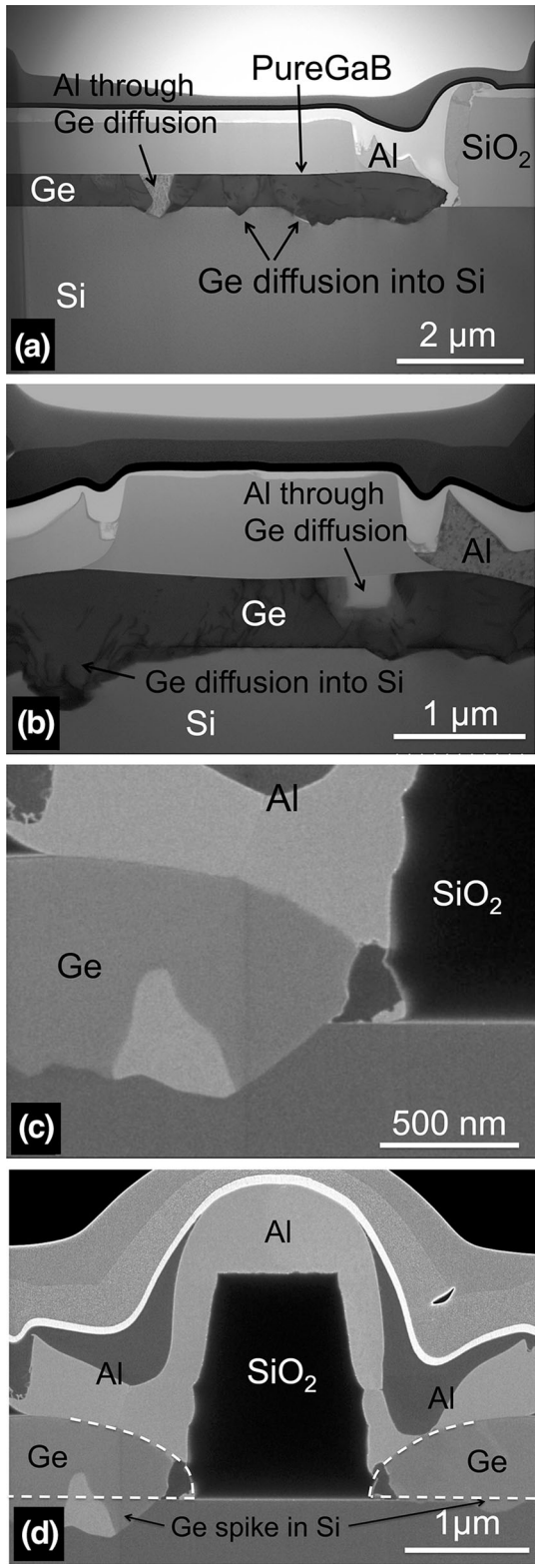

Fig. 4. TEM images of Ge-on-Si diodes fabricated as in Fig. 1b with oxide light-entrance windows and Al-contacting at the perimeter for diodes of (a) size 26 μm^2 $\times$ 26 μm^2, and (b, c, d) size 5 μm^2 $\times$ 5 μm^2. In (c) and (d), close-ups are shown of the tips of the Ge islands where Al contacts the Ge through 1-μm-wide contact windows. In (d), the white-dashed lines indicate the expected original shapes of two Ge islands separated by an oxide hill before the processing of the contacts.

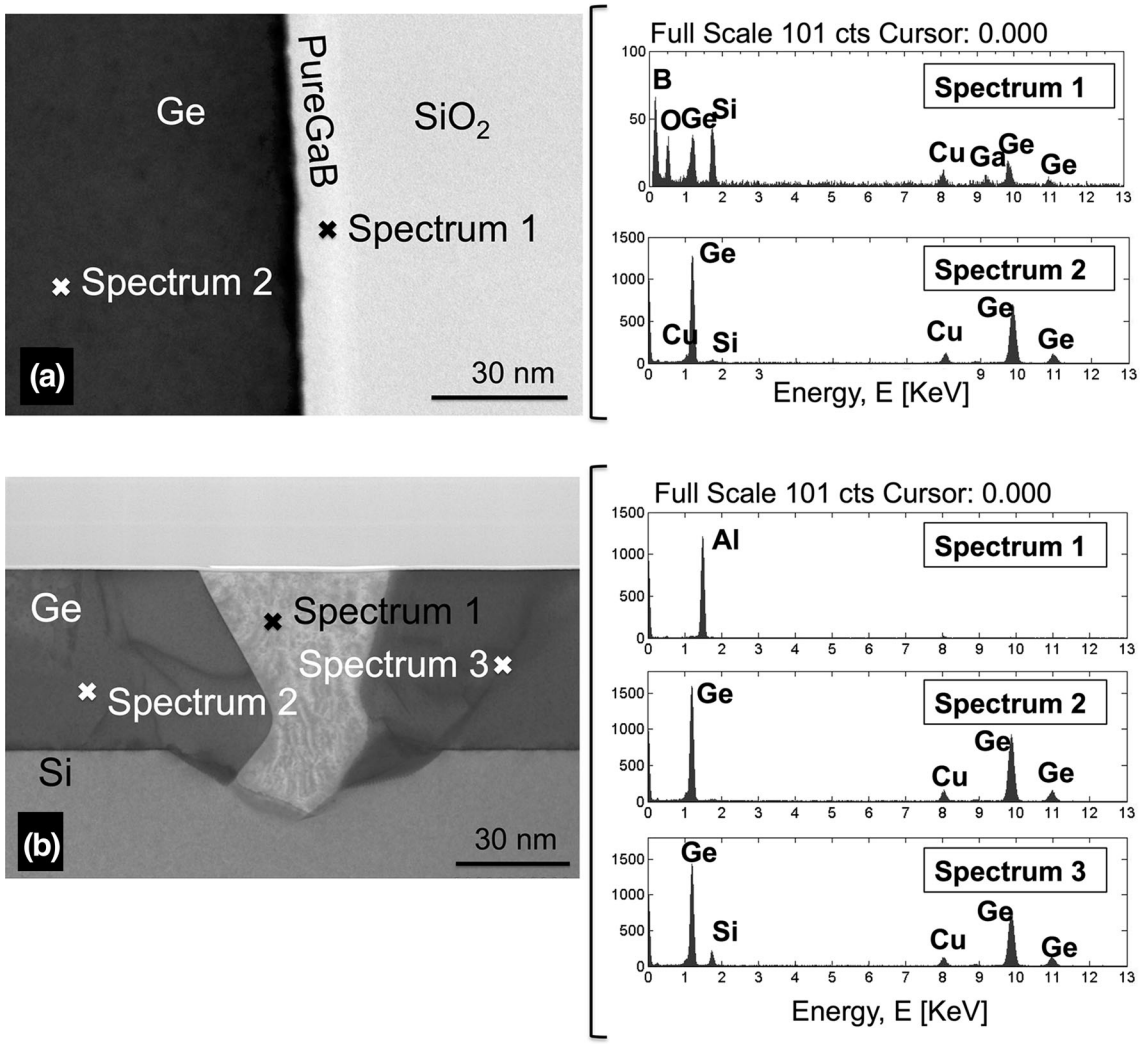

Fig. 5. Cross-sectional TEM images of the same devices as shown in Fig. 4 along with EDS analysis. (a) A TEM of PureGaB on Ge covered with PECVD SiO_2 and 2 EDS spectra taken on the PureGaB and inside the Ge island. (b) A TEM of the region where an Al grain has formed in the Ge and 3 EDS spectra taken on this grain as well as in the surrounding Ge and on one of the misfit dislocations.

reveals that the oxide has been etched down to the bulk Si. This means that the tip of the Ge, otherwise covered by oxide, is then exposed to the Al. From this tip, Ge has migrated toward the central diode region. Pure Al is known to cause spiking in Si, which should be prevented by the use of Al/Si(1%). Nevertheless, in this case, the Al migration through the Ge also results in Si removal leaving V-grooves that are filled with Ge. In Fig. 4d, a dashed line is drawn where it is plausible to assume that the as-grown Ge crystal was formed. In all the available TEMs, a shape like this is easily identified.

An EDS analysis of the different regions resulting from the Al migration is shown in Fig. 5a for the PureGaB layer on top of the Ge and in Fig. 5b for a region inside the Ge. In the spectra, C and Cu are system artifacts. The C is attributed to residual vacuum pump oils and the Cu to the Cu grid on which the sample was mounted. The traces of Si and O in the PureGaB layer in spectrum 1 of Fig. 4a come from the top SiO_2 layer. In Fig. 4b, the spectra 2 and 3 show no trace of Al, B, or Ga in the Ge surrounding the Al grain that, from the spectrum 1, is found to be quite pure. The spectrum 2 of Fig. 4b shows a barely discernible trace of Si, while spectrum 3 taken at a misfit dislocation network shows a small but significant peak of Si. Although these TEM images do not reveal any Si precipitates, it cannot be excluded that they may have formed elsewhere. It may also be because the Si is absorbed by defects in the Ge and in small amounts in the Al. In any case, it is clear that all three materials are migrating, while the PureGaB, which also can be discerned in Fig. 4d where the oxide was removed, remains intact and forms a barrier to the Al which contacts the Ge via the PureGaB over most of the 1-μm-wide contact window. The PureGaB plus the oxide are apparently mechanically strong enough to

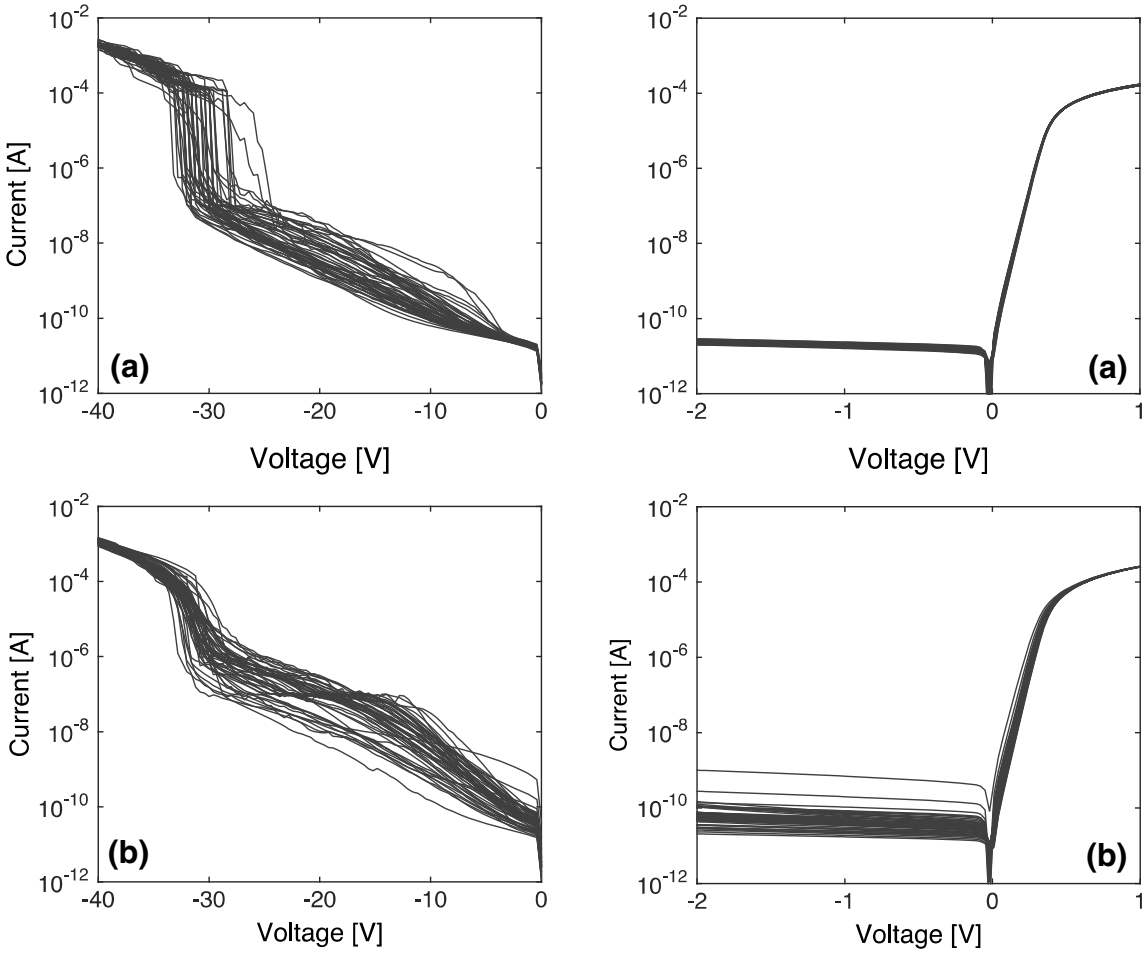

Fig. 6. The *I–V* characteristics of the 16-diode device for (left) reverse and (right) forward biases for 50 devices measured on dies either (a) at the center or (b) at the bottom of the wafer.

maintain the upper topography of the Ge crystal. In cases where the oxide is removed in the contact but PureGaB is preserved, some very small dents are visible, but still the basic form of the crystal is maintained. Therefore, Ge can only be consumed at the perimeter tip of the crystal.

A statistical analysis of the diode *I–V* characteristics was made on the wafer from which the TEM devices also were taken. Two tendencies were identified, and they are illustrated in Fig. 5 for the 16-diode devices. In all, 50 devices were measured within each 1 mm^2 × 1 mm^2 die. In the central part of the wafer when measured from −2 V to 1 V, the I_{on}/I_{off} ratio was 10^7 and the current spread was very low: 25 pA ± 5 pA at 2.0 V reverse-bias. The corresponding high-voltage reverse current was low and characterized by a delayed breakdown around 30 V. This ability to bias past the breakdown point without actually inducing breakdown indicates that this type of diode is suitable for SPAD operation as already demonstrated in Ref. 7. On the bottom part of the wafer, the diodes displayed higher dark current with a spread of up to a decade in saturation current, and the breakdown is characterized by gradual avalanching as would be suitable for avalanche photodiode (APD) operation. In Fig. 6, the trend over the wafer for diodes with the lowest saturation current places the lowest current in the center/top region. Both the oxide deposition and etching steps could give such a distribution, which indicates that it is process related rather than due to random defects. Thus, it can be optimized by investing in the process control and monitoring.

The single-diode and 4-diode devices showed the same trends as the 16-diode devices. The lowest measured current values found among the measured devices at bias voltages of 0.2 V and −2 V are compared in Table I for each type of device. The current level follows the total area rather than the total perimeter length. The series resistance attenuating the forward current is about 3000 Ω for all devices and dominated by the resistance through the wafer. Therefore, the contact resistance must be much lower than this since it should be three times higher for the single-diode device compared to the 16-diode device. The ideality factor is approximately 1.05 in almost all cases, so the higher current found for some devices could possibly be related to the

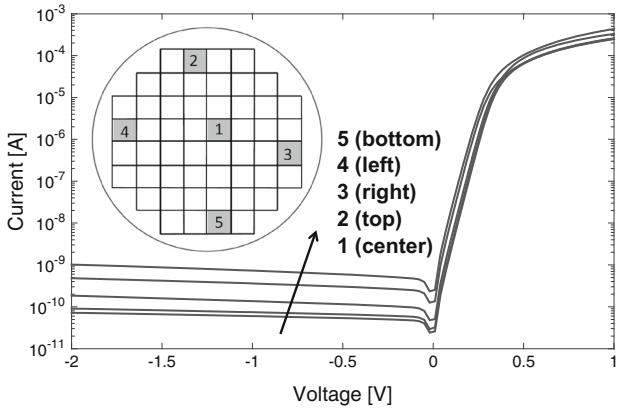

Fig. 7. The *I–V* characteristics of the single-diode devices at 5 different positions on the wafer. The characteristic with the lowest saturation current among 50 measured devices is shown.

formation of Al-Ge Schottky diodes around the Al grains formed in the Ge, rather than being related to defects in the Ge. Since the TEMs are taken at the center of the wafer where the *I–V* characteristics are the best, it is likely that all devices on the wafer were affected by Al migration through the Ge crystal. The low series resistance also supports this because contacting through 10-nm PureB would otherwise give high contact resistance in the kΩ range.[25] The lower series resistance, higher current levels, and spread at the bottom of the wafer as shown in Fig. 7b, all suggest a more aggressive etching in this region with more Al diffusion into the Ge as a result.

A detailed electrical and optical characterization of these devices[18] shows a performance that demonstrates Ge-enhanced NIR response. For example, at a temperature of 77 K and a wavelength of 940 nm, an average quantum efficiency of 18% and a maximum optical gain in avalanche mode of operation of $\sim 10^6$ were found.

CONCLUSIONS

The use of PureB as an interdiffusion barrier to Al was studied for application in PureGaB Ge-on-Si photodiodes. It proves to be an excellent barrier but if incomplete, like in the contacting process described here, Al-mediated material transport can derange the device structure and electrical functioning. The specific case studied here is seen to form a special situation where the restricted nature of the Al supply allows for significant lateral material migration, but it is not destructive in terms of the ideality and yield of the diode *I–V* characteristics. Over the main surface of the Ge islands where the PureGaB is left intact, the PureB is seen to form an efficient interdiffusion barrier completely preventing Al-spiking of the Ge. Together with the oxide coverage of the PureGaB, a rigid layer is formed, which preserves the surface morphology of the Ge-island despite the Al-mediated material displacement. At the perimeter where contacts are made, TEM analysis shows that the Ge island edge is exposed to the Al, and in our process, this leads to Al migration up to 5 μm laterally through the Ge crystal. In this process, Ge and Si are displaced, and the migrating Al coalesces into grains. For measurements over arrays of photodiodes, an increase in current levels with a spread of no more than a decade is observed. The formation of a small volume of Al-Ge Schottky diodes at the coalesced Al grains could account for the increased saturation currents. This process did not destroy the diode ideality and compared to other Ge diode processes, the currents are still low with acceptable spread for many applications. In the whole central part of the wafers, the spread in saturation current is extremely small: for example, 25 pA ± 5 pA at 2.0 V reverse-bias for the 16-diode devices with an individual diode size of 5 $\mu m^2 \times 5$ μm^2. Overall, the results indicate that with optimization of the across-the-wafer control of the contact etching process, the presented process flow is suitable for high-yield fabrication of PureGaB Ge photodiodes with oxide light-entrance windows, and excellent uniformity of characteristics with low contact resistance, low dark current, and breakdown behavior suitable for either APD or SPAD operation.

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